Amendments to the Specification:

1. Please replace the title "METHOD OF CORRECTING A MASK LAYOUT" with the following new title:

--METHOD OF CORRECTING CRITICAL DIMENSIONS OF ELEMENT PATTERNS ON A WAFER--

2. Please replace paragraph [0002] with the following amended paragraph:

[0002] The present invention relates to a method of correcting critical dimensions of element patterns on a wafer ~~a mask layout~~, and more particularly, to a method of correcting systematic errors produced during a pattern transfer process on element patterns on a wafer ~~a mask layout~~.

3. Please replace paragraph [0004] with the following amended paragraph:

[0004] To form a designed integrated circuit (IC) on a semiconductor wafer, a semiconductor foundry forms a mask with a designed layout pattern and then performs a photolithographic process to transfer the designed layout pattern on the mask to a photoresist layer positioned on a semiconductor wafer. [[.]] Following this, an etching process is performed using the photoresist layer as an etching mask, transferring patterns of the photoresist layer to the semiconductor wafer. The photolithographic process and the etching process are apparently the most important steps for determining the IC patterns during the

semiconductor manufacturing process

4. Please replace paragraph [0005] with the following amended paragraph:

[0005] However, during the photolithographic process, a pattern transferring deviation occurs due to [[an]] overexposure or [[an]] underexposure at corners of the closely arranged mask patterns. [[As]] Being non-uniformly exposed, an optical proximity effect occurs, [[to]] affecting the pattern transferring precision on the photoresist layer. To prevent the optical proximity effect from affecting the pattern transferring precision, a solution is [[using]] to use a computer aided design (CAD) system to provide an optical proximity correction (OPC) on the mask patterns.

5. Please replace paragraph [0007] with the following amended paragraph:

[0007] Please refer to Fig.1, which shows a mask layout according to the prior art. The mask layout includes a plurality of linear element patterns A, B, and C for defining conductive areas, such as word lines or bit lines. The element patterns A, B, and C have an equal line width w. A line space [[s]] between two element patterns A is defined as a, a line space [[s]] between two element patterns B is defined as b, and a line space [[s]] between two element patterns C is defined as c. The line spaces a, b, and c are not equal, and the pattern densities of the element patterns A, B, and C on the mask layout are therefore considered different.

6. Please replace paragraph [0008] with the following amended paragraph:

[0008] Next, please refer to Fig.2, which shows a relationship between an etched line width w and a line space [[s]] between the element patterns on the mask layout. The vertical axis of the relation diagram represents an after-etch-inspection (AEI) critical dimension of an element pattern's line width[[,]]. The horizontal axis of the relation diagram represents a line space between two element patterns of the mask layout. The circles represent experimental values of the etched line width, and the solid line represents a fitting curve of the experimental values of the etched line width. As shown in Fig.2, since a value of the etched line width w changes as a result of a micro-loading effect or other systematic errors, different etched line widths w are achieved for the element patterns having different pattern densities. For example, when the etched line width increases with an increase in the line space between two adjacent element patterns, a greater etched line width is achieved for the isolated element patterns, and a narrower etched line width is achieved for the dense element patterns

7. Please replace paragraph [0009] with the following amended paragraph:

[0009] For an integrated circuit with design rules of 0.18 μm, micro-loading effect is mildly regarded [[slight]] since it is not a subject factor to affect etching uniformity of a semiconductor wafer. However, when the design rules of the semiconductor elements lower to 0.15 μm, 0.13 μm, or even 0.1 μm, a 10 nm line width deviation creates an error percentage of 6%, 8%, or even 10%. Therefore, improvement in surface uniformity has become an important issue for the manufacturing process, especially for the design rules of below 0.15 μm.

8. Please replace paragraph [0010] with the following amended paragraph:

[0010] It is an objective of the claimed invention to provide a method of correcting critical dimensions of element patterns on a wafer ~~a mask layout~~ to effectively prevent micro-loading effect from inducing pattern transferring deviations.

9. Please replace paragraph [0011] with the following amended paragraph:

[0011] According to the claimed invention, ~~a mask layout including a plurality of element patterns is provided. An~~ an inspection program is executed to classify [[the]] element patterns of [[the]] a mask layout into a plurality of element pattern types according to pattern deviation data of transferred element patterns onto a wafer ~~a pattern density of the element patterns~~. Following this, each of the element pattern types is corrected and transferred to the wafer so as to prevent a plasma micro-loading effect.

10. Please replace paragraph [0015] with the following amended paragraph:

[0015] Fig.2 is a ~~schematic diagram for~~ chart illustrating a relationship between an etched line width and a line space of a mask layout according to the prior art.

11. Please replace paragraph [0021] with the following amended paragraph:

[0021] As the micro-loading effect is resulted from different pattern densities of the element patterns, a step 20 of the present invention provides an inspection program to classify the element patterns into a plurality types according to their pattern densities. For example, as shown in step 30, the element patterns are divided into four types of element patterns 32, 34, 36, and 38 after ~~classifying~~classification. The element patterns 32, 34, 36, and 38 have different pattern densities and are called dense patterns, sub-dense patterns, semi-dense patterns, and isolated patterns, respectively.

12.Please replace paragraph [0026] with the following amended paragraph:

[0026] In the preferred embodiment, the pattern density is determined by a distance between two adjacent line patterns. For example, for the element patterns A, B, and C, a pattern density order of these three element patterns is determined by the values of the line spaces a, b, and c. In addition, the pattern density can be determined by other ways [[which]] that can distinguish dense patterns from isolated patterns, such as dividing a line width of an element pattern by a line space between this element pattern and an adjacent element pattern. For example, the pattern density d between two element patterns A is calculated with the following equation: d=w/a; wherein w represents a line width of the element pattern A, and a represents a line space between two adjacent element patterns A.

13.Please replace abstract of the present application with the following amended paragraph:

A method of correcting critical dimensions of element patterns on a wafer ~~a mask layout~~ is provided. ~~The mask layout includes a plurality~~

~~of element patterns.~~ An inspection program is executed to classify [[the]] element patterns of [[the]] a mask layout into a plurality of element pattern types according to pattern deviation data of transferred element patterns onto the wafer ~~a pattern density of the element patterns~~. Following this, each of the element pattern types is corrected and transferred to the wafer so as to prevent a plasma micro-loading effect.